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TITLE: SEMICONDUCTOR DEVICE AND METHOD OF PRODUCING SAME

Hon. Commissioner for Patents,
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SIR;

CERTIFIED TRANSLATION

I, Yasuo OKUZAWA, am an official translator of the Japanese language into the English language and I hereby certify that the attached comprises an accurate translation into English of Japanese Application No. 2003-120393, filed on April 24, 2003.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

December. 14, 2005 Yasuo Okuzawa

Date Yasuo OKUZAWA

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[TITLE OF THE INVENTION] Semiconductor Device and Method of Producing Same

[CLAIMS]

[Claim 1]

A semiconductor device comprising:

a semiconductor mesa portion formed on a substrate, including a stack of at least a collector layer, a base layer, and an emitter layer formed in a narrower region compared with said base layer, and functioning as an active region of a bipolar transistor;

a base contact pad mesa portion formed on said substrate apart from said semiconductor mesa portion and formed with a same height as a height of a top surface of said base layer; and

a conductive layer formed integrally with a base electrode formed and connected to said base layer at part of a formation region of said base layer other than a formation region of said emitter layer, a base contact pad electrode formed on said base contact pad mesa portion in a region other than near edges of a top surface of said base contact pad mesa portion, and an interconnection portion for connecting said base electrode and said base contact pad electrode.

[Claim 2]

A semiconductor device as set forth in claim 1, wherein a surface layer of said base contact pad mesa portion is formed by the same layer as said base layer.

[Claim 3]

A semiconductor device as set forth in claim 1, wherein an area under said conductive layer between said semiconductor mesa portion and said base contact pad mesa portion forms a space.

[Claim 4]

A semiconductor device as set forth in claim 1, wherein an insulation film is formed under said conductive layer between said semiconductor mesa portion and said base contact pad mesa portion.

[Claim 5]

A semiconductor device as set forth in claim 1, wherein said base electrode is formed in a region other than a formation region of said emitter layer and other than a region near an edge of said base layer.

[Claim 6]

A semiconductor device as set forth in claim 1, wherein a distance between said semiconductor mesa portion and said base contact pad mesa portion is 1 to 5 μm.

[Claim 7]

A semiconductor device as set forth in claim 1,

wherein said semiconductor mesa portion is formed by a stack of compound semiconductors and has a heterojunction bipolar transistor.

[Claim 8]

A method of producing a semiconductor device having a bipolar transistor including an emitter layer, a base layer and a collector layer on a substrate, comprising the steps of:

forming a stack of at least the collector layer, the base layer, and the emitter layer on the substrate;

patterning said stack to form, separated with a predetermined distance, a semiconductor mesa portion including a stack of at least the collector layer, the base layer, and the emitter layer formed in a narrower region than said base layer and functioning as an active region of a bipolar transistor and a base contact pad mesa portion having a same height as a height of a top surface of said base layer and having a surface layer formed by the same layer as said base layer;

forming, between said semiconductor mesa portion and said base contact pad mesa portion, a covering layer having a top surface higher than a height of the top surface of said base layer on said substrate and covering a region at least up to near an edge of a top surface of said base contact pad mesa portion; and

forming a conductive layer on said covering layer by using said covering layer as a mask and integrally forming a base electrode connected to said base layer at part of a formation region of said base layer other than a formation region of said emitter layer, a base contact pad electrode on said base contact pad mesa portion in a region other than near edges of the top surface of said base contact pad mesa portion, and an interconnection portion connecting said base electrode and said base contact pad electrode.

[Claim 9]

A method of producing a semiconductor device as set forth in claim 8, further comprising the step of removing said covering layer after the step of forming said conductive layer.

[Claim 10]

A method of producing a semiconductor device as set forth in claim 8, wherein the step of forming said covering layer comprises forming said covering layer by an insulation film.

[Claim 11]

A method of producing a semiconductor device as set forth in claim 8, wherein:

the step of forming said covering layer comprises forming said layer to cover a region up to near the edge

of said base layer of said semiconductor mesa portion; and

the step of forming said conductive layer comprises forming said base electrode in a region other than the formation region of said emitter layer and other than near the edge of said base layer.

[Claim 12]

A method of producing a semiconductor device as set forth in claim 8, comprising forming said semiconductor mesa portion by a compound semiconductor to form a heterojunction bipolar transistor.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor device having bipolar transistors and a method of producing the same, more particularly relates to a semiconductor device having heterojunction bipolar transistors and a method of producing the same.

[0002]

[Prior Art]

The transistors used for semiconductor devices may be roughly divided into bipolar transistors and field effect transistors such as a metal oxide semiconductor (MOS) field effect transistor.

[0003]

One type of the bipolar transistors is a heterojunction bipolar transistor (hereinafter, referred to an HBT).

Nonpatent Document 1 discloses a base electrode takeout portion capable of lowering a capacity between a base and a collector of an InP/InGaAs-based HBT.

FIG. 8A is a plane view illustrating such an HBT, and FIG. 8B is a cross-sectional view along the line X-X' of FIG. 8A.

A substrate 100 of InP has a sub-collector layer 101 of an n^+-type InGaAs and forming a collector takeout layer, a collector layer 102 of an n^--type InGaAs, a base layer 103 of a p^+-type InGaAs, an emitter layer 104 of an n-type InP, an emitter cap layer (not shown) of an n^+-type InP and InGaAs, etc. successively stacked on each other.

[0004]

An emitter electrode 105 is formed connected to the emitter cap layer. For forming a base contact, the emitter cap layer and the emitter layer 104 are removed in part to form an emitter mesa portion EM.

A base electrode 106a is formed connected to the base layer 113. The base layer 103 and the collector layer 102 are formed with a base mesa portion BM.

The sub-collector layer 101 is formed with a sub-collector mesa portion SM, while a collector electrode 107 is formed connected to the sub-collector layer 101.

[0005]

At a position separated with a predetermined distance from an edge (an end portion) of the base mesa portion BM, a base contact pad base mesa portion PBM including a layer 101a of the same layer as the sub-collector layer 101, a layer 102a of the same layer as the collector layer 102, and a layer 103a of the same layer as the base layer 103 is formed.

The base contact pad base mesa portion PBM is formed with a base contact pad electrode 106b.

Here, the base layer 103 formed under the base electrode 106a and the layer 103a formed under the base contact pad electrode 106b were originally the same layer, so the heights of surfaces of the above two layers are the same, and the base electrode 106a and the base contact pad electrode 106b are connected by an interconnection portion 106c.

The area under the conductive layer 106 and between the base mesa portion BM and the base contact pad base mesa portion PBM forms a space SP. The interconnection portion 106c is formed to float above the space.

[0006]

The heterojunction bipolar transistor HBT is formed as described above. An insulation film 108 is formed to cover the entire HBT. The insulation film 108 is formed with an emitter contact hole CHe reaching the emitter electrode 105, a base contact hole CHb reaching the base contact pad electrode 106b, and a collector contact hole CHc reaching the collector electrode 110.

The emitter contact hole CHe is formed with an emitter contact plug interconnection 109e connected with the emitter electrode 105.

The base contact hole CHb is formed with a base contact plug interconnection 109b connected with the base contact pad electrode 106b.

The collector contact hole CHc is formed with a collector contact plug interconnection 109c connected with the collector electrode 110.

[0007]

Here, a drawn direction DR of the interconnection portion 106c is for example made the [001] direction or the [010] direction of an InP crystalline orientation of the substrate due to the following production reasons.

[0008]

A method of producing the HBT will be described with reference to the drawings.

As shown in FIG. 9A, the substrate 100 of InP is

successively formed with, by a molecular beam epitaxy (MBE) or a metal organic chemical vapor deposition (MOCVD), the n^+-type InGaAs as the sub-collector layer 101, the n^--type InGaAs as the collector layer 102, the p^+-type InGaAs as the base layer 103, the n-type InP as the emitter layer 104, and the n^+-type InP and InGaAs as the emitter cap layer (not shown).

Next, a resist film (not shown) is formed in the pattern of the emitter mesa portion EM. The film is used as a mask for etching to process the emitter cap layer (not shown) and the emitter layer 105 to the emitter mesa portion EM and to expose a surface of the base layer 103.

[0009]

As shown in FIG. 9B, by vapor deposition of a conductive layer for example by using the lift-off method, the emitter electrode 105 is formed and the conductive layer 106 of the base electrode 106a, the base contact pad electrode 106b, and the interconnection portion 106c is formed.

Here, the conductive layer 106 is arranged such that the interconnection portion 106c extends in the [001] direction or the [010] direction of the InP crystalline orientation of the substrate 100 as shown in FIG. 8A.

[0010]

As shown in FIG. 10A, the resist film 107 is formed in the pattern of the base mesa portion BM.

[0011]

As shown in FIG. 10B, the base layer 103 and the collector layer 102 are etched by using the resist film 107 as a mask to form the base mesa portion BM. Another resist film (not shown) is formed in the pattern of the sub-collector mesa portion SM. The film is used as a mask for etching to process the sub-collector layer 101 to the sub-collector mesa portion SM to thereby isolate elements.

By using an enchant of a type having an anisotropic etching property where side etching greatly proceeds in a direction perpendicular to the [001] direction or the [010] direction of the InP crystalline orientation, the sub-collector layer 101, the collector layer 102, and the base layer 103 under the interconnection portion 106c are completely removed.

In the above case, under the base contact pad electrode 106b, the layer 101a formed by the same layer as the sub-collector layer 101, the layer 102a formed by the same layer as the contact layer 102, and the layer 103a formed by the same layer as the base layer 103 are left, whereby a base contact pad base mesa portion PBM is formed. Side etching proceeds somewhat due to the above-mentioned side-etching property, so a base contact pad

base mesa portion PBM is formed in a narrower region compared with a formation region of the base contact pad electrode 106b.

[0012]

As subsequent steps, the collector electrode 107 is formed by vapor deposition for example using the lift-off method, the insulation film 108 is formed by CVD etc., a resist film is formed in a pattern of the contact holes, and the insulation film 108 is etched by using the resist film as a mask by reactive ion etching (RIE) to open the emitter contact hole CHe, the base contact hole CHb, and the collector contact hole CHc. The contact plug interconnection 109e, the contact plug interconnection 109b, and the contact plug interconnection 109c are formed in the contact holes to form the structure shown in FIG. 8A and FIG. 8B.

[0013]

[Nonpatent Document 1]

IEICE Technical Report, ED99-262 (Institute of Electronics, Information and Communication Engineers)

[0014]

[Problem to be Solved by the Invention]

The above-mentioned method of producing a semiconductor device of the related art however suffers from disadvantages that there are restrictions on the

drawn direction of the interconnection portion 106c and types of enchant used in etching for removing completely the sub-collector layer 101, the collector layer 102, and the base layer 103 under the interconnection portion 106c.

In etching for forming the above base mesa portion, if the closeness of adhesion of the metal conductive layer 106 and a resist film formed on the step differences of the epitaxially grown semiconductor layer is insufficient, the enchant will invade along the step differences to cause a mesa portion-shaped abnormality.

[0015]

The present invention was made in consideration of the above situations, an object of the present invention is to provide a semiconductor device free of the restrictions on the pattern layout or the types of etchant to be used and able to be produced while suppressing mesa portion-shaped abnormalities and a method of producing the same.

[0016]

[Means for Solving the Problem]

To achieve the above object, according to a first aspect of the present invention, there is provided a semiconductor device having a semiconductor mesa portion formed on a substrate, including a stack of at least a collector layer, a base layer, and an emitter layer

formed in a narrower region compared with the base layer, and functioning as an active region of a bipolar transistor; a base contact pad mesa portion formed on the substrate apart from the semiconductor mesa portion and formed with a same height as a height of a top surface of the base layer; and a conductive layer formed integrally with a base electrode formed connected to the base layer at part of a formation region of the base layer other than a formation region of the emitter layer, a base contact pad electrode formed on the base contact pad mesa portion in a region other than near edges of a top surface of the base contact pad mesa portion, and an interconnection portion for connecting the base electrode and the base contact pad electrode.

[0017]

The semiconductor device of the present invention has a configuration in which the base contact pad electrode is taken out from the base electrode through the interconnection portion and has the conductive layer formed integrally with the base electrode formed connected to the base layer at part of the formation region of the base layer other than the formation region of the emitter layer, the base contact pad electrode formed on the base contact pad mesa portion, and the interconnection portion for connecting the base electrode

and the base contact pad electrode.

Here, the base contact pad electrode is formed at the region other than near edges of the top surface of the base contact pad mesa portion.

[0018]

According to a second aspect of the invention, there is provided a method of producing a semiconductor device having a bipolar transistor including an emitter layer, a base layer and a collector layer on a substrate, having the steps of forming a stack of at least the collector layer, the base layer, and the emitter layer on the substrate; patterning the stack to form, separated with a predetermined distance, a semiconductor mesa portion including a stack of at least the collector layer, the base layer, and the emitter layer formed in a narrower region than the base layer and functioning as an active region of a bipolar transistor and a base contact pad mesa portion having the same height as a height of a top surface of the base layer and having a surface layer formed by the same layer as the base layer; forming, between the semiconductor mesa portion and the base contact pad mesa portion, a covering layer having a top surface higher than the height of the top surface of the base layer on the substrate and covering a region at least up to near an edge of a top surface of the base

contact pad mesa portion; and forming a conductive layer on the covering layer by using the covering layer as a mask and integrally forming a base electrode connected to the base layer at part of a formation region of the base layer other than a formation region of the emitter layer, a base contact pad electrode on the base contact pad mesa portion in a region other than near edges of the top surface of the base contact pad mesa portion, and an interconnection portion connecting the base electrode and the base contact pad electrode.

[0019]

In the method of producing a semiconductor device of the present invention, the stack of at least the collector layer, the base layer, and the emitter layer is formed on the substrate.

Then, the stack is patterned to form, separated with a predetermined distance, a semiconductor mesa portion including the stack of at least the collector layer, the base layer, and the emitter layer formed in the narrower region than the base layer and functioning as the active region of the bipolar transistor and the base contact pad mesa portion having the same height as the height of the top surface of the base layer and having the surface layer formed by the same layer as the base layer.

Then, the covering layer having the top surface higher than the height of the top surface of the base layer on the substrate and covering a region at least up to near the edge of the top surface of the base contact pad mesa portion is formed between the semiconductor mesa portion and the base contact pad mesa portion.

Then, the conductive layer is formed on the covering layer by using the covering layer as a mask (mold) to integrally form the base electrode connected to the base layer at part of the formation region of the base layer other than the formation region of the emitter layer, the base contact pad electrode on the base contact pad mesa portion at a region other than near edges of the top surface of the base contact pad mesa portion, and the interconnection portion connecting the base electrode and the base contact pad electrode.

[0020]

[Embodiments of the Invention]

Hereinafter, a semiconductor device and a method of producing the same will be explained with reference to the drawings.

[0021]

First Embodiment

FIG. 1A is a plane view of a semiconductor device including a heterojunction bipolar transistor according

to a first embodiment, and FIG. 1B is a cross-sectional view along the line X-X' of FIG. 1A.

A semiinsulating substrate 10 of an Fe-doped single crystal InP has successively formed on it with a sub-collector layer 11 of a thickness of about 500 nm of an n^+-type InP, a collector layer 12 of a thickness of about 500 nm of an n^--type InP, a base layer 13 of a p^+-type InGaAs, an emitter layer 14 of a thickness of about 75 nm of an n-type InP, and an emitter cap layer (not shown) of a thickness of about 75 nm of an n^+-type InGaAs and functions as an active region of the heterojunction bipolar transistor.

The sub-collector layer 11 includes a higher concentration of conductive impurities than the collector layer 12 and forms a collector takeout layer.

[0022]

An emitter electrode 15 is formed connected to the emitter cap layer. For forming a base contact, the emitter cap layer and the emitter layer 14 are removed in part to form an emitter mesa portion EM.

A base electrode 17a is formed connected to the base layer 13, while the base layer 13 and the collector layer 12 are formed with a base mesa portion BM.

The sub-collector layer 11 is formed with a sub-collector mesa portion SM (an isolation mesa portion for

isolating elements), and a collector electrode 18 is formed connected to the sub-collector layer 11.

[0023]

At predetermined distance of for example 1 to 5 μm away from the end of the base mesa portion BM, a base contact pad base mesa portion PBM having a layer 12a of the same layer as the collector layer 12 and a layer 13a of the same layer as the base layer 13 is formed. Under this portion, a base contact pad sub-collector mesa portion PSM having a layer 11a of the same layer as the sub-collector layer is formed.

Therefore, a height of a top surface of the base contact pad base mesa portion PBM becomes the same as a height of a top surface of the base mesa portion BM.

[0024]

The base contact pad electrode 17b is formed on the base contact pad base mesa portion PBM.

Here, the base layer 13 under the base electrode 17a and the layer 13a under the base contact pad electrode 17b are originally formed by the same layer and are the same height in the top surfaces. The base electrode 17a and the base contact pad electrode 17b are connected by an interconnection portion 17c, which forms a base electrode takeout portion for reducing the base-collector capacity.

The area between the base mesa portion BM and the base contact pad base mesa portion PBM and under the conductive layer 17 forms a space 16a. Namely, the interconnection portion 17c floats above this.

The base contact pad base mesa portion PBM and the sub-collector mesa portion PSM are electrically insulated from a transistor part and other elements by the semiinsulating substrate 10, so the capacities of these parts do not become the parasitic capacitance of the transistor.

[0025]

The emitter electrode 15, the conductive layer 17 including the base electrode 17a, and the collector electrode 18 are formed by a stack of Ti/Pt/Au for example.

[0026]

Here, the base contact pad electrode 17b is formed in a region other than near edges PBMa of a top surface of the base contact pad mesa portion of the base mesa portion PBM. For example, it is formed in a region inside from the edge PBMa of the top surface of the base contact pad base mesa portion PBM in a range of about 0.5 to 2 μm.

On the other hand, the base electrode 17a is formed in a region other than the formation region of the emitter layer 14 and other than a region near the edge

portion 13b of the base layer 13. For example, it is formed in a region inside from the edge 13b of the base layer 13 in a range of about 0.5 to 2 μm.

[0027]

The heterojunction bipolar transistor HBT is formed as described above. An insulation film 19 is formed to cover the entire HBT. The insulation film 19 is formed with an emitter contact hole CHe reaching the emitter electrode 15, a base contact hole CHb reaching the base contact pad electrode 17b, and a collector contact hole CHc reaching the collector electrode 18.

The emitter contact hole CHe is formed with an emitter contact plug interconnection 20e connected with the emitter electrode 15.

The base contact hole CHb is formed with a base contact plug interconnection 10b connected with the base contact pad electrode 17b.

The collector contact hole CHc is formed with a collector contact plug interconnection 20c connected with the collector electrode 18.

[0028]

The semiconductor device having the HBT according to the present embodiment is configured provided with an external takeout contact pad from the base electrode without increasing the base-collector capacity and can

prevent a degradation of the high frequency properties of the devices.

The height of the top surface of the base contact pad base mesa portion PBM is the same as that of the base mesa portion BM, so it is possible to form an air bridge at the interconnection portion for taking out the base with a good shape.

[0029]

The base contact pad electrode 17b is formed in the region other than near the edges PBMa of the top surface of the base contact pad mesa portion of the base mesa portion PBM. The base electrode 17a is formed in a region other than the formation region of the emitter layer 14 and other than near the edge 13b of the base layer 13. As later description, by the method of forming a resist film or other covering layer between the base contact pad mesa portion and the base mesa portion and forming a conductive layer by using this as a mask (mold), it may be possible to easily form the base contact pad electrode 17b and the base electrode 17a of the above structure. By using this method for production, it is possible to eliminate the restrictions on the pattern layout, the types of the etchant used, etc., suppress the occurrence of mesa portion-shaped abnormalities, and maintain the shape of the mesa etching well for production.

[0030]

Since the base mesa portion BM and the base contact pad base mesa portion PBM are separately arranged in 1 to 5 μm, the device area of the HBT can be reduced.

The thickness of the interconnection portion 17c is a thin one of about 0.2 to 0.5 μm, as a result the strength thereof is insufficient, so if increasing a distance, the interconnection portion 17c may be liable to be damaged. To prevent this, it is preferable to set the distance between the base mesa portion BM and the base contact pad base mesa portion PBM to the above range.

[0031]

The method of producing the semiconductor device having the HBT according to the present embodiment will be explained with reference to the drawings.

As shown in FIG. 2A, the semiinsulating substrate 10 of Fe-doped single crystal InP is successively formed with, by the MBE or the MOCVD, the n^+-type InGaAs as the sub-collector layer 11, the n^--type InP as the collector layer 12, the p^+-type InGaAs as the base layer 13, the n-type InP as the emitter layer 14, and the n^+-type InGaAs as the emitter cap layer (not shown).

[0032]

Next, as shown in FIG. 2B, the emitter electrode 15 is formed on the emitter layer 15 by for example the

lift-off method etc.

A not shown resist film used for patterning the emitter electrode 15 or the emitter electrode 15 etc. is used as a mask to successively process the emitter cap layer and the emitter layer 14 to emitter mesa portion EM.

As a result, the surface of the base layer 13 is exposed.

In the above-mentioned etching, the InGaAs of the emitter cap layer is etched by using a mixture of phosphoric acid, hydrogen peroxide, and water as the etchant, while the InP of the emitter layer is etched by using a mixture of hydrochloric acid and phosphoric acid.

[0033]

Next, as shown in FIG. 3A, a resist film (not shown) is formed in the pattern of the base mesa portion BM and the base contact pad base mesa portion PBM. The resist film is used as a mask for etching to process the base layer 13 and the collector layer 12 to the base mesa portion BM. Simultaneously, the layer 12a formed by the same layer as the collector layer 12 and the layer 13a formed by the same layer as the base layer 13 are patterned as the base contact pad base mesa portion PBM.

In the same way as the above, the InGaAs of the base layer 13 for example is etched by using a mixture of phosphoric acid, hydrogen peroxide, and water, while the

InP of the collector layer 12 is etched by using a mixture of hydrochloric acid and phosphoric acid.

[0034]

Next, as shown in FIG. 3B, a resist film (not shown) is formed in a pattern of the sub-collector portion SM and the base contact pad sub-collector mesa portion PSM. The resist film is used as a mask for etching to process the sub-collector layer 11 to the sub-collector mesa portion SM to thereby isolate the elements. Simultaneously, the layer 11a of the same layer as the sub-collector layer 11 is patterned to form the base contact pad sub-collector mesa portion PSM.

In the same way as the above, the InGaAs of the sub-collector layer 11 is for example etched by using a mixture of phosphoric acid, hydrogen peroxide, and water.

[0035]

In the above way, the semiconductor mesa portion of the emitter mesa portion EM, the base mesa portion BM, and the sub-collector mesa portion SM functioning as the active region of the heterojunction bipolar transistor and the base contact pad mesa portion of the base mesa portion PBM and the sub-collector mesa portion PSM having the same height as the top surface of the base layer and having a surface layer formed by the same layer as the base layer, are separately formed with a predetermined

distance.

[0036]

Next, as shown in FIG. 4A, between the semiconductor mesa portion of the emitter mesa portion EM, the base mesa portion BM, and the sub-collector mesa portion SM and the base contact pad mesa portion of the base mesa portion PBM and sub-collector mesa portion PSM, the resist film 16 is patterned on the substrate 10 as a covering layer having a top surface higher than the height of the top surface of the base layer 13 so as to cover a region at least up to near the edges PBMa of the top surface of the base contact pad base mesa portion PBM (the region of about 0.5 to 2 μm from the edges PBMa) and cover a region up to near the edge 13b of the base layer 13 (the region of about 0.5 to 2 μm from the edge 13b).

[0037]

Next, as shown in FIG. 4B, for example vapor deposition using the lift-off method etc. is used to form the conductive layer 17 of a thickness of about 0.2 to 0.5 μm on the resist film 16 by using the resist film 16 as a mask (mold).

Namely, the base electrode 17a connected to the base layer at part of the region other than the formation region of the emitter layer 14 and other than near the edge 13b of the base layer 13, the base contact pad

electrode 17b on the base contact pad base mesa portion in the region other than near the edges PBMa of the top surface thereof, and the interconnection portion 17c connecting the base electrode 17a and the base contact pad electrode 17b are integrally formed.

[0038]

Next, as shown in FIG. 5A, the resist film 16 is removed.

As a result, the area under the conductive layer 17 and between the semiconductor mesa portion of the emitter mesa portion EM, the base mesa portion BM, and the sub-collector mesa portion SM and the base contact pad mesa portion of the base mesa portion PBM and the sub-collector mesa portion PSM forms a space 16a, as a result, an air bridge structure is formed.

[0039]

Next, as shown in FIG. 5B, the collector electrode 18 is formed on the sub-collector layer 11 by vapor deposition using for example the lift-off method.

The heterojunction bipolar transistor HBT is formed by the above process.

[0040]

As shown in FIG. 6A, for example, CVD is used to deposit silicon oxide over the entire surface and covering the entire HBT to form the insulation film 19.

In the above case, sometimes part of the insulation film may be formed sneaking into the space 16a under the interconnection portion 17c, but it is possible to prevent the film from sneaking into and leave the space as it is depending on the film-forming conditions.

[0041]

As shown in FIG. 6B, the insulation film 19 formed by CVD etc. is formed on its surface with a resist film having the pattern of the contact holes, and is etched by reactive ion etching (RIE) to form the emitter contact hole CHe, the base contact hole CHb, and the collector contact hole CHc.

As subsequent steps, the contact holes are formed with the contact plug interconnection 20e, the contact plug interconnection 20b, and the contact plug interconnection 20c.

The semiconductor device having the HBT of the same structure as that shown in FIG. 1A and FIG. 1B can be produced.

[0042]

According to the method of producing a semiconductor device of the present embodiment, since the height of the top surface of the base contact pad base mesa portion PBM is the same as that of the base mesa portion BM, it is possible to form an air bridge of the

interconnection portion for taking out the base in a good shape.

Further, since the mesa shape is formed without etching utilizing the side etching property based on the crystalline orientation of the substrate, then the conductive layer 17 integrally formed of the base electrode 17a, the base contact pad electrode 17b, and the interconnection portion 17c is formed, there is no restriction on the pattern layout and the types of the etchant used, etc. In etching for forming the base mesa portion, the etching may be performed in the state with no step difference possibly causing mesa shape abnormalities to suppress the occurrence of mesa shape abnormalities and keep the shape of the mesa etching good in the producing the device.

[0043]

Second Embodiment

FIG. 7 is a cross-sectional view of a semiconductor device having a heterojunction bipolar transistor according to a second embodiment of the present invention.

The semiconductor device of the second embodiment is similar to the semiconductor device of the first embodiment, but differs in the point that an insulation film 16b such as silicon oxide is formed in the space formed under the conductive layer 17 and between the

semiconductor mesa portion of the emitter mesa portion EM, the base mesa portion BM, and the sub-collector mesa portion SM and the base contact pad mesa portion of the base mesa portion PBM and the sub-collector mesa portion PSM.

[0044]

Since a silicon oxide or other insulation film has a dielectric constant higher than air, the electrostatic capacity of this portion rises somewhat in the semiconductor device according to the present embodiment. In the same way as the first embodiment, as description later, by forming an insulation film of silicon oxide or other covering layer between the base contact pad mesa portion and the base mesa portion and forming a conductive layer by using the insulation film as a mask (mold), the base contact pad electrode 17b and the base electrode 17a of the above structure can be formed easily. Since this method is used for a production, the production is possible while eliminating the restrictions on the pattern layout and the types of the etchant used etc. and suppressing the occurrence of mesa shape abnormalities.

[0045]

The semiconductor device according to this embodiment can be produced in substantially the same way

as the first embodiment.

Namely, in the step of forming the resist film 16 as a covering layer in the first embodiment, the insulation film 16b of silicon oxide for example is formed as the covering layer. In the step of forming the conductive layer 17 on the covering layer by using the covering layer as a mask (mold), the conductive layer is formed on the insulation film 16b by using the insulation film 16b as a mask (mold). By leaving the film 16b and performing the following steps in the same way as the first embodiment, it is possible to form the structure shown in FIG. 7.

[0046]

According to the method of producing the semiconductor device of the present embodiment, in the same way as the first embodiment, since there is no etching utilizing the side-etching property based on the crystalline orientation of the substrate, there is no restriction on the pattern layout and the types of etchant used etc. In etching for forming a base mesa portion, the etching can be performed in a state with no step difference possibly causing mesa portion-shaped abnormalities, so the occurrence of mesa portion-shaped abnormalities can be suppressed.

[0047]

The present invention is not limited to the above embodiments.

For example, in the above embodiments, the base mesa portion PBM and the sub-collector mesa portion PSM are used as the base contact pad mesa portion, but the invention is not limited thereto. It is also possible to form a new mesa portion for the base contact pad. Note that, the above case may be needed that the height of the top surface of the base contact pad mesa portion is designed to become the same height as that of the base layer.

Further, the base electrode 17a is not necessarily formed in the region other than the formation region of the emitter layer 14 and other than near the edge 13b of the base layer 13. It may be sufficient that at least the base contact pad electrode 17b is formed in a region other than near the edges PBMa of the top surface of the base mesa portion PBM of the base contact pad mesa portion. Note that, the structure may be easily produced by also forming the base electrode 17a in a region other than near the edge 13b of the base layer 13.

[0048]

Further, in the above embodiments, the explanation was given with reference to an npn-type bipolar transistor, but the invention can also be applied to a

pnp-type bipolar transistor.

Further, the shapes of the mesa portion of the stack of the collector layer, the base layer, and the emitter layer and the arrangement of the electrodes connected to the different layers etc. are not limited to the above embodiments. Other shapes and arrangements may also be adopted.

In addition, the present invention is not limited to an application to the heterojunction bipolar transistor and may be applied to semiconductor devices having other bipolar transistors as well.

[0049]

[Effect of the Invention]

The semiconductor device of the present invention can be produced without restrictions as to the pattern layout the types of etchant used etc. and while suppressing mesa portion-shaped abnormalities.

[0050]

According to the method of producing a semiconductor device of the present invention, it is possible to produce a semiconductor device without restrictions as to the pattern layout, the types of etchant used, etc. and while suppressing mesa shape abnormalities.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1]

FIG. 1A is a plane view of a semiconductor device including a heterojunction bipolar transistor according to a first embodiment of the present invention, and FIG. 1B is a cross-sectional view along line X-X' of FIG. 1A.

[FIG. 2]

FIGs. 2A and 2B are cross-sectional views of steps of a method of producing the semiconductor device including a heterojunction bipolar transistor according to the first embodiment.

[FIG. 3]

FIGs. 3A and 3B are cross-sectional views of steps of the method of producing the semiconductor device including the heterojunction bipolar transistor according to the first embodiment.

[FIG. 4]

FIGs. 4A and 4B are cross-sectional views of steps of the method of producing the semiconductor device including the heterojunction bipolar transistor according to the first embodiment.

[FIG. 5]

FIGs. 5A and 5B are cross-sectional views of steps of the method of producing the semiconductor device including the heterojunction bipolar transistor according to the first embodiment.

[FIG. 6]

FIGs. 6A and 6B are cross-sectional views of steps of the method of producing the semiconductor device including the heterojunction bipolar transistor according to the first embodiment.

[FIG. 7]

FIG. 7 is a plane view of a semiconductor device including a heterojunction bipolar transistor according to a second embodiment of the present invention.

[FIG. 8]

FIG. 8A is a cross-sectional view of a semiconductor device including a heterojunction bipolar transistor according to the prior art, and FIG. 8B is a cross-sectional view along line X-X' of FIG. 8A.

[FIG. 9]

FIGs. 9A and 9B are cross-sectional views of steps of a method of producing a semiconductor device including a heterojunction bipolar transistor according to the prior art.

[FIG. 10]

FIGs. 10A and 10B are cross-sectional views of steps of the method of producing the semiconductor device including the heterojunction bipolar transistor according to the prior art.

[Description of References]

10...substrate, 11...sub collector layer, 12...collector layer, 13...base layer, 14...emitter layer, 15...emitter electrode, 16...resist film (covering layer), 16a...space, 16b...insulation film (covering layer), 17...conductive layer, 17a...base electrode, 17b...base contact bad electrode, 17c...interconnection portion, 18...collector electrode, 19...insulation film, 20e, 20b, 20c...contact plug interconnection, 11a...layer formed by the same layer as the sub collector layer, 12a... layer formed by the same layer as the collector layer, 13a... layer formed by the same layer as the base layer, CHe, CHb, CHc...contact hole, EM...emitter mesa portion, BM...base mesa portion, SM...sub collector mesa portion, PBM...base contact pad base mesa portion, PSM...base contact pad sub collector mesa portion.

FIG. 1A

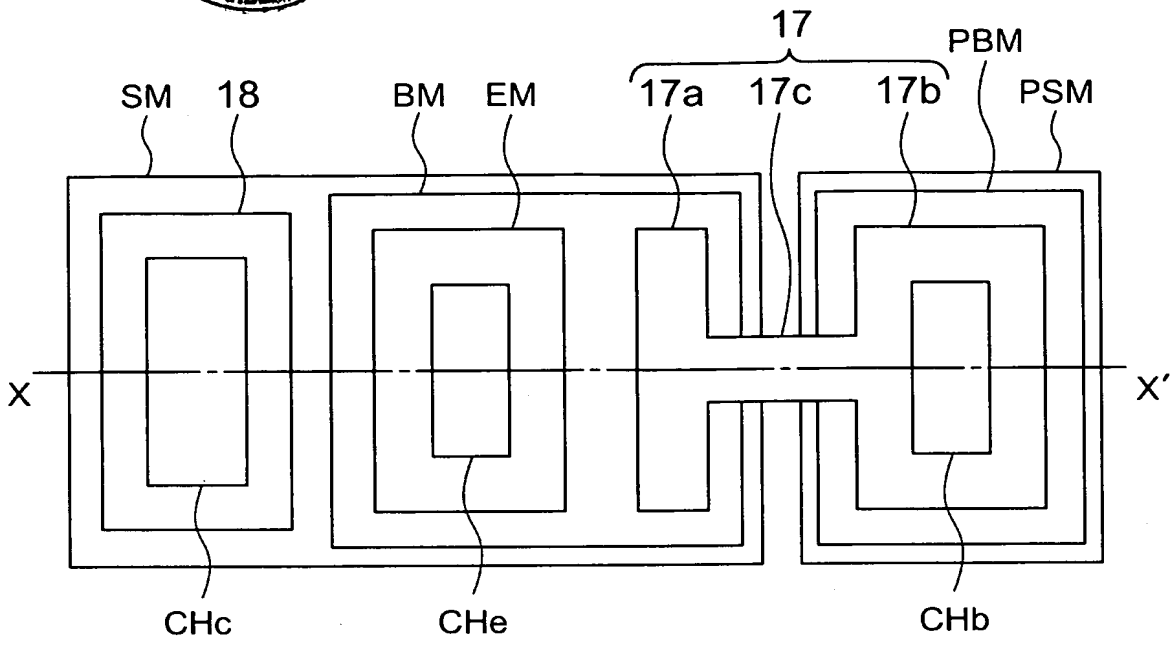
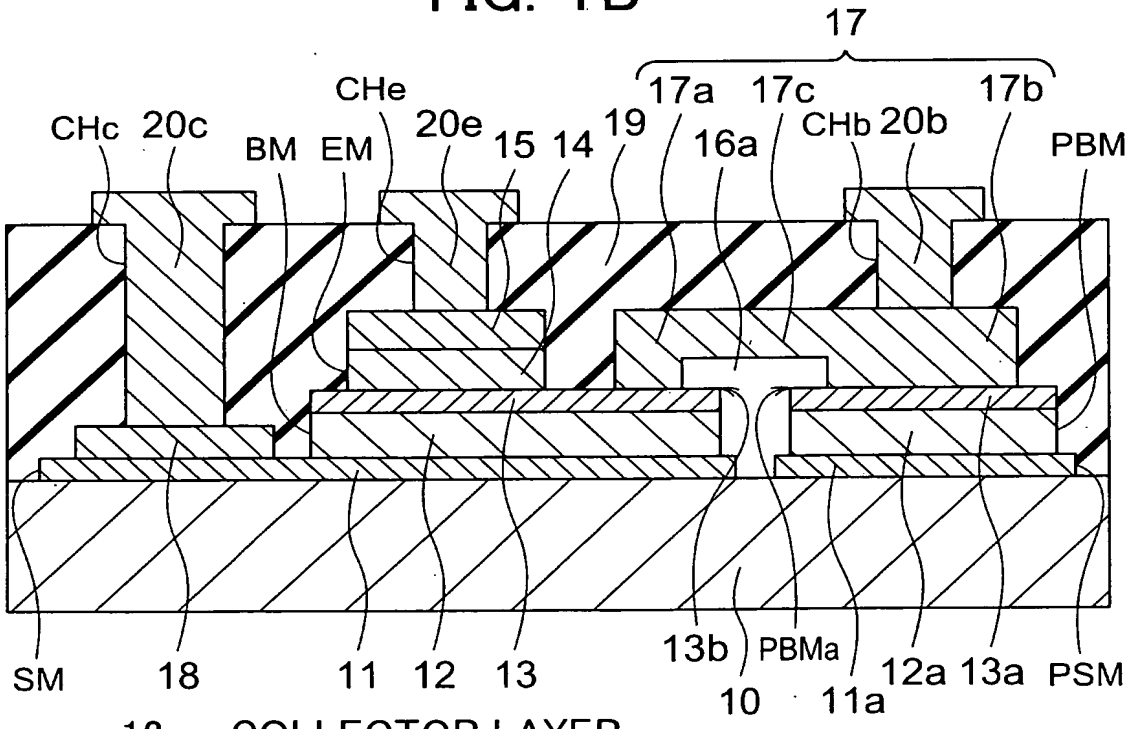


FIG. 1B



12･･･COLLECTOR LAYER
13･･･BASE LAYER
14･･･EMITTER LAYER
17･･･CONDUCTIVE LAYER
17a･･･BASE ELECTRODE
17b･･･BASE CONTACT PAD ELECTRODE
17c･･･INTERCONNECTION PORTION
BM･･･BASE MESA PORTION
PBM･･･BASE CONTACT PAD BASE MESA PORTION

FIG. 2A

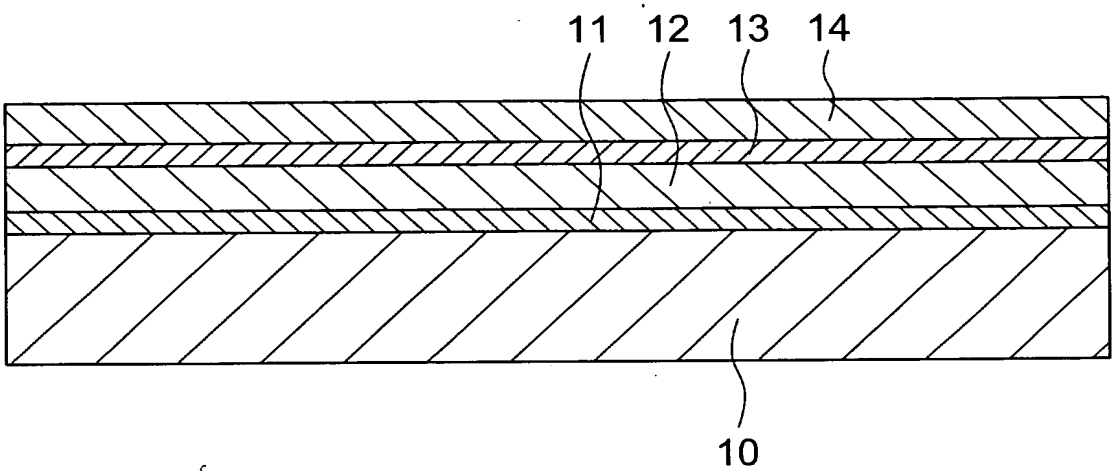


FIG. 2B

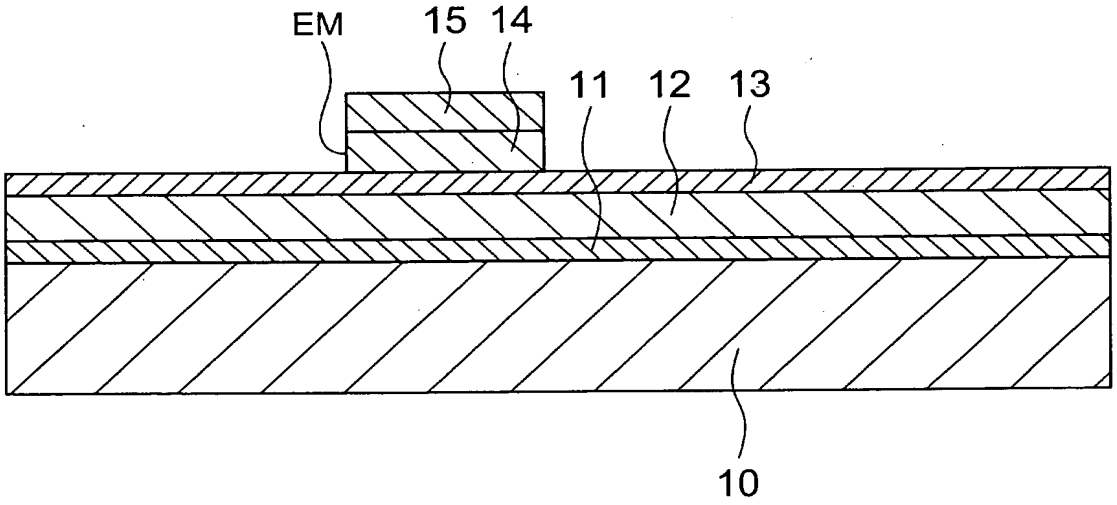


FIG. 3A

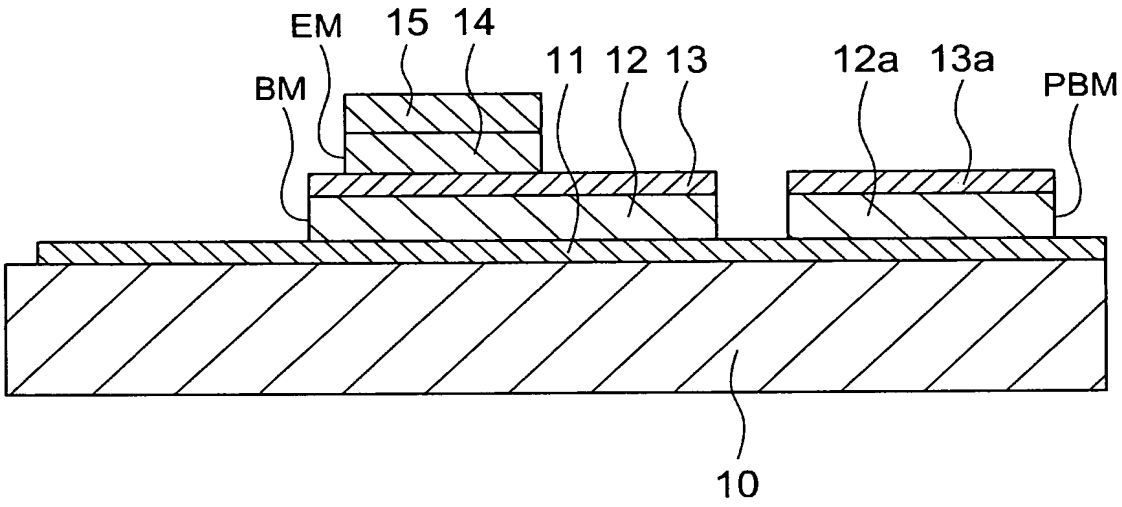

EM
15
14
11
12
13
12a
13a
PBM
BM
10

FIG. 3B

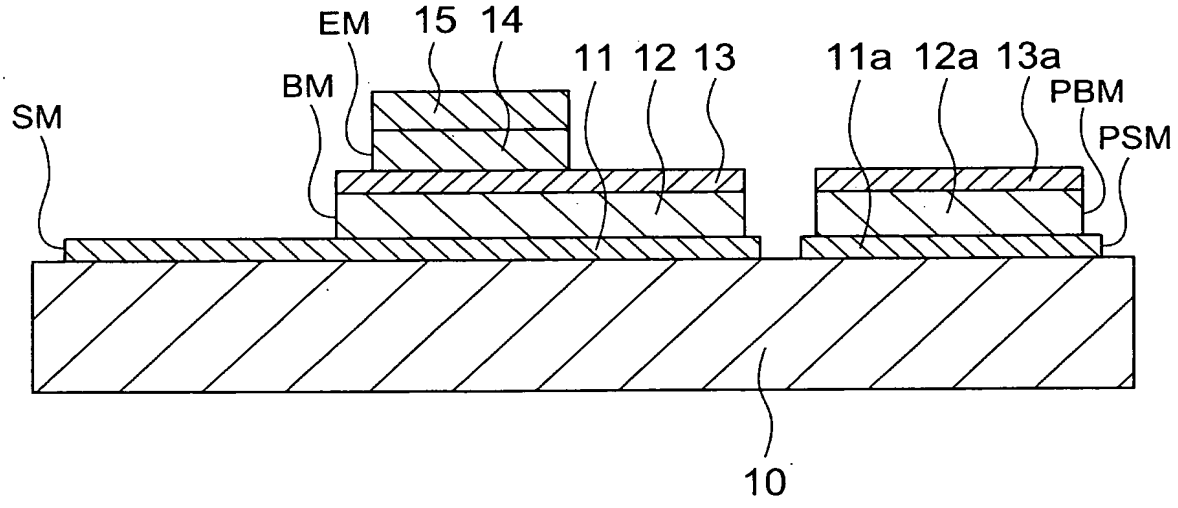

EM
15
14
11
12
13
11a
12a
13a
PBM
PSM
BM
SM
10

FIG. 4A

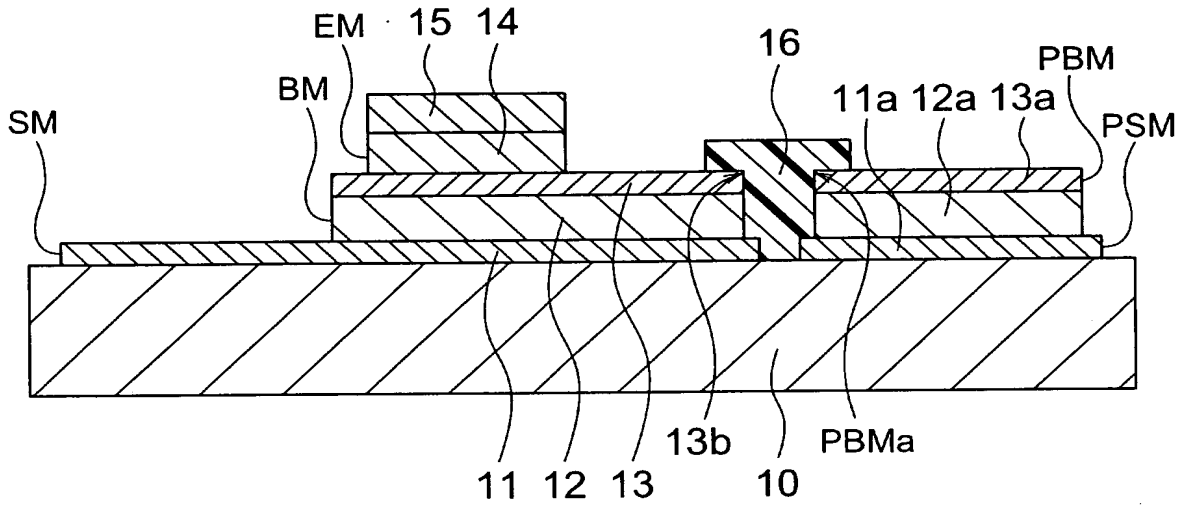

EM
15
14
16
PBM
BM
11a
12a
13a
SM
PSM
11
12
13
13b
10
PBMa

FIG. 4B

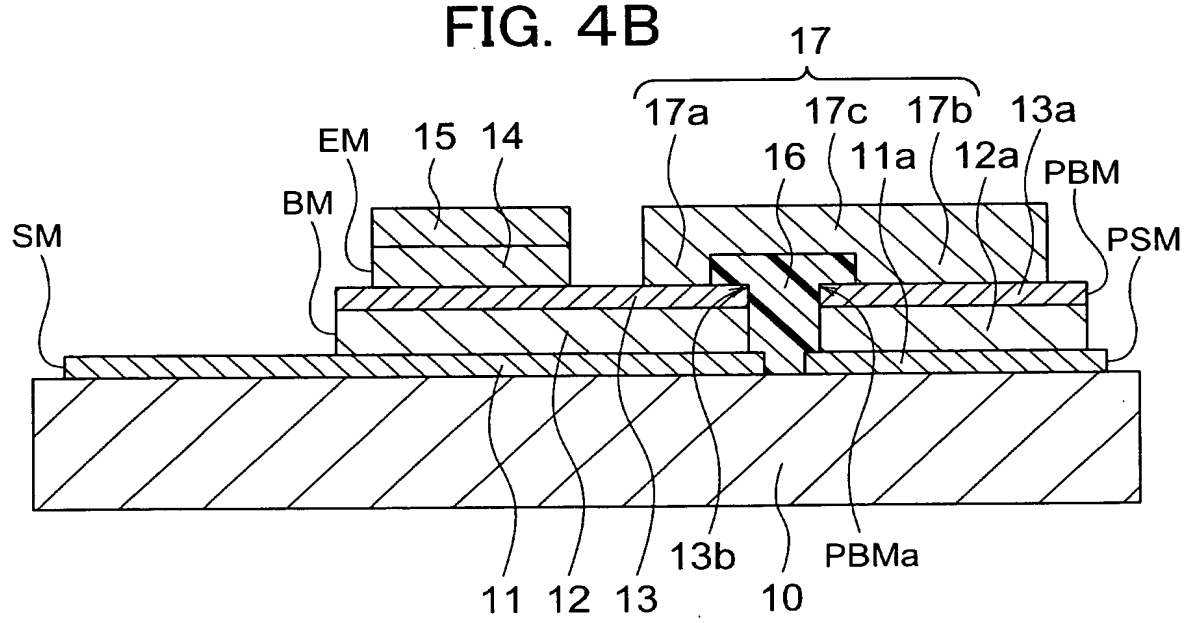

17
17a
17c
17b
13a
EM
15
14
16
11a
12a
PBM
BM
SM
PSM
11
12
13
13b
10
PBMa

FIG. 5A

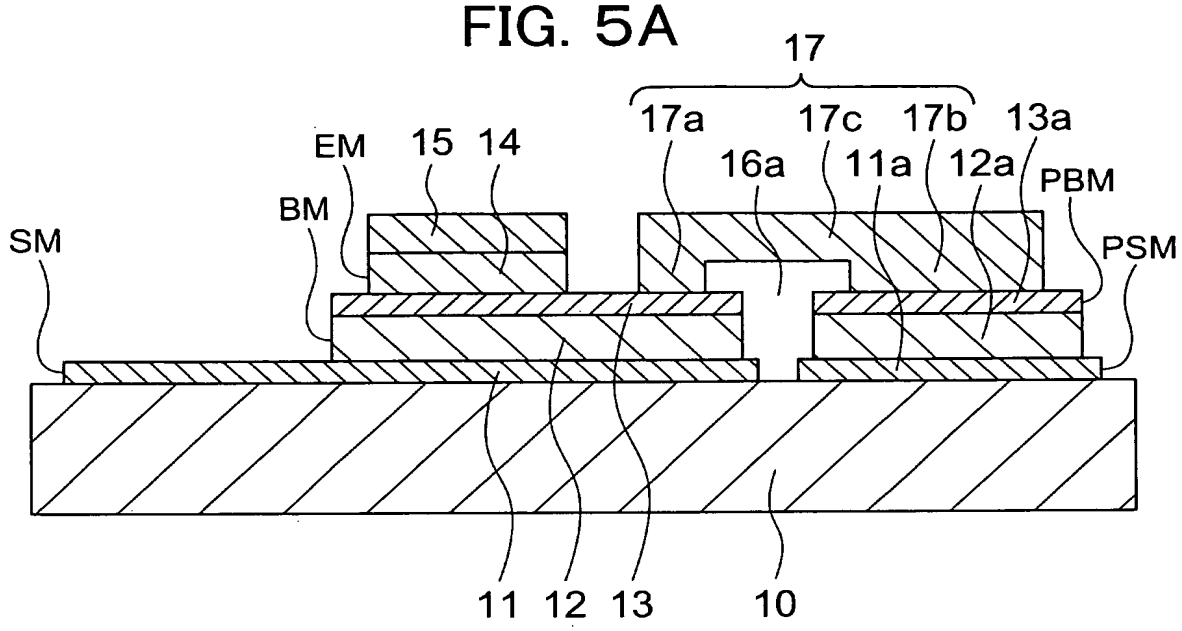

17
17a
17c
17b
13a
EM
15
14
16a
11a
12a
PBM
BM
SM
PSM
11
12
13
10

FIG. 5B

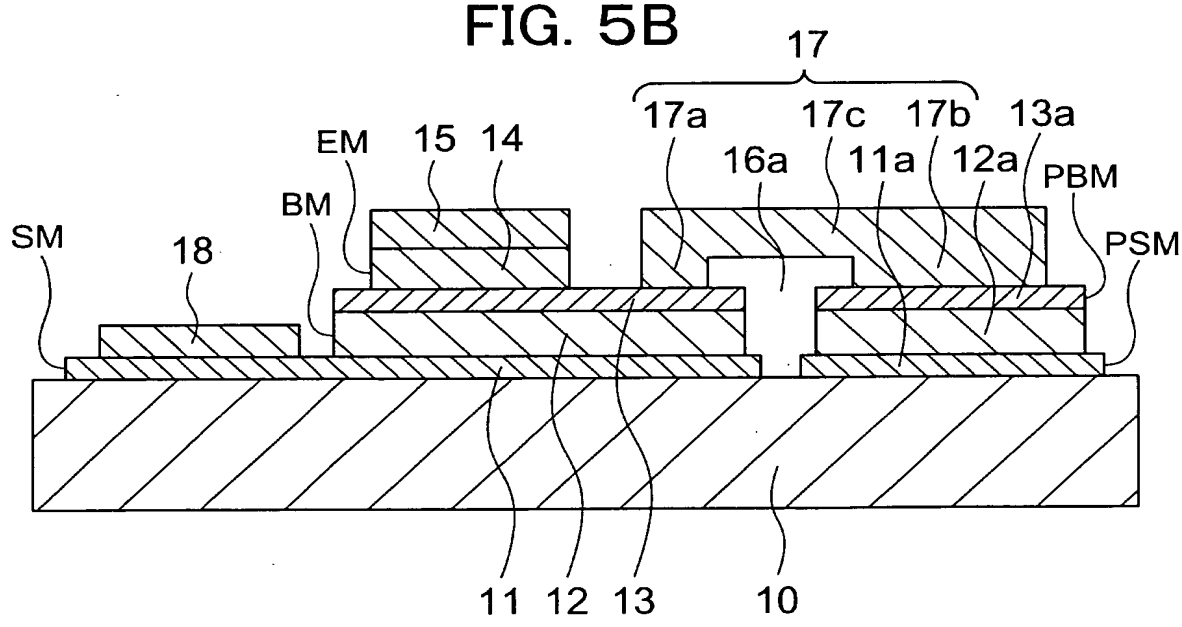

17
17a
17c
17b
13a
EM
15
14
16a
11a
12a
PBM
BM
SM
18
PSM
11
12
13
10

FIG. 6A

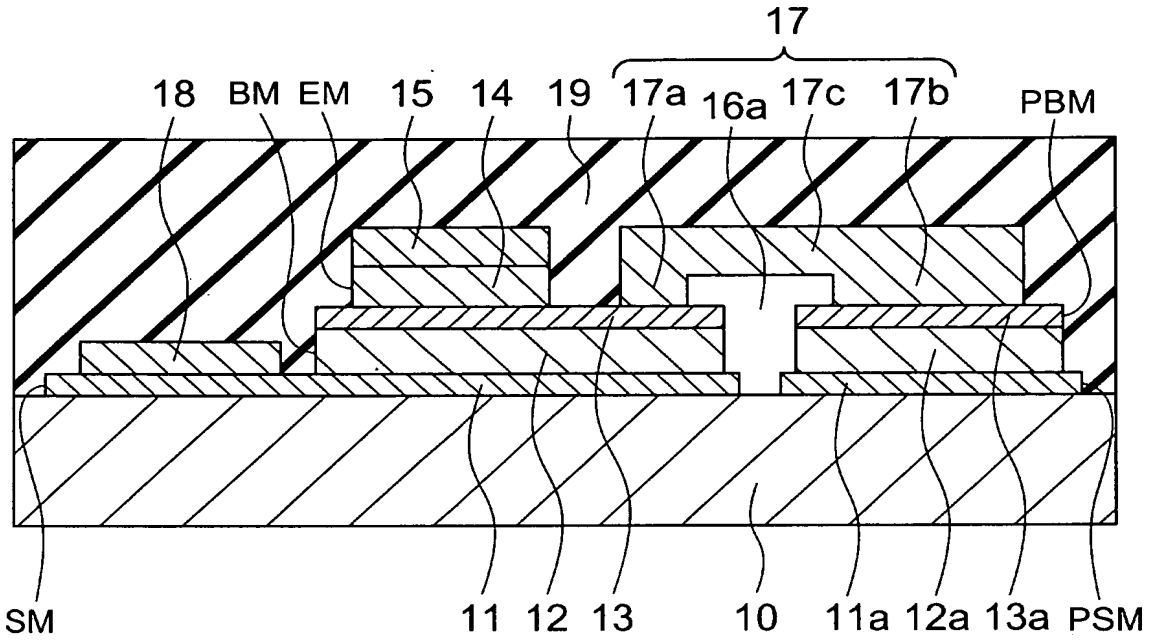

17
18
BM
EM
15
14
19
17a
16a
17c
17b
PBM
SM
11
12
13
10
11a
12a
13a
PSM

FIG. 6B

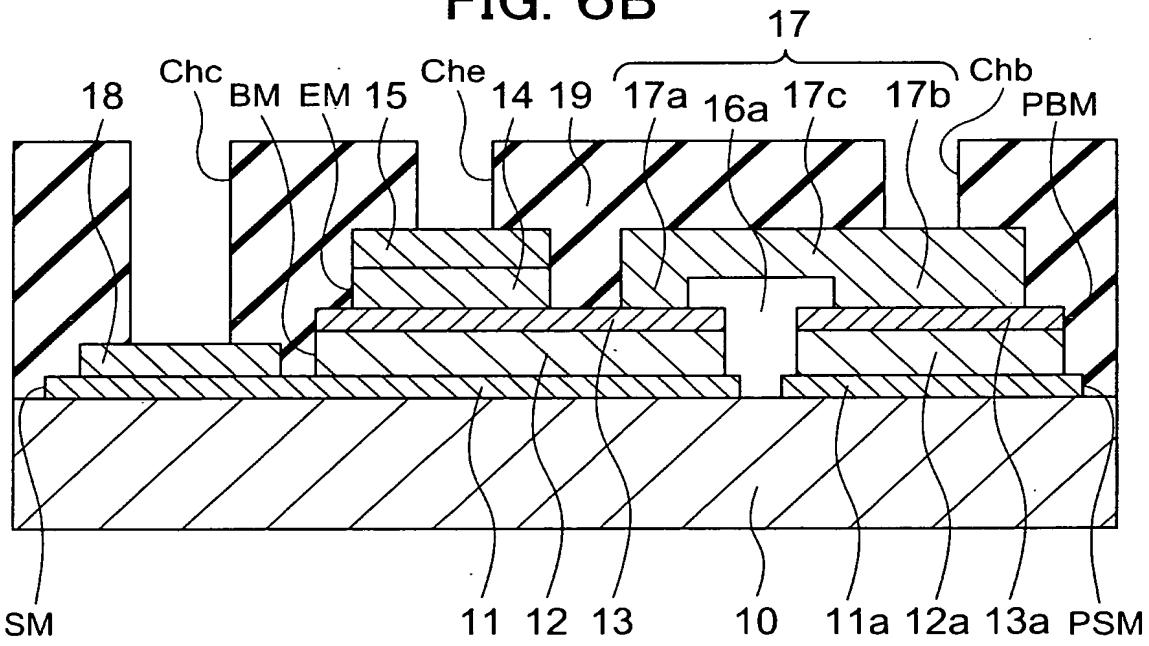

17
18
Chc
BM
EM
15
Che
14
19
17a
16a
17c
17b
Chb
PBM
SM
11
12
13
10
11a
12a
13a
PSM

FIG. 7

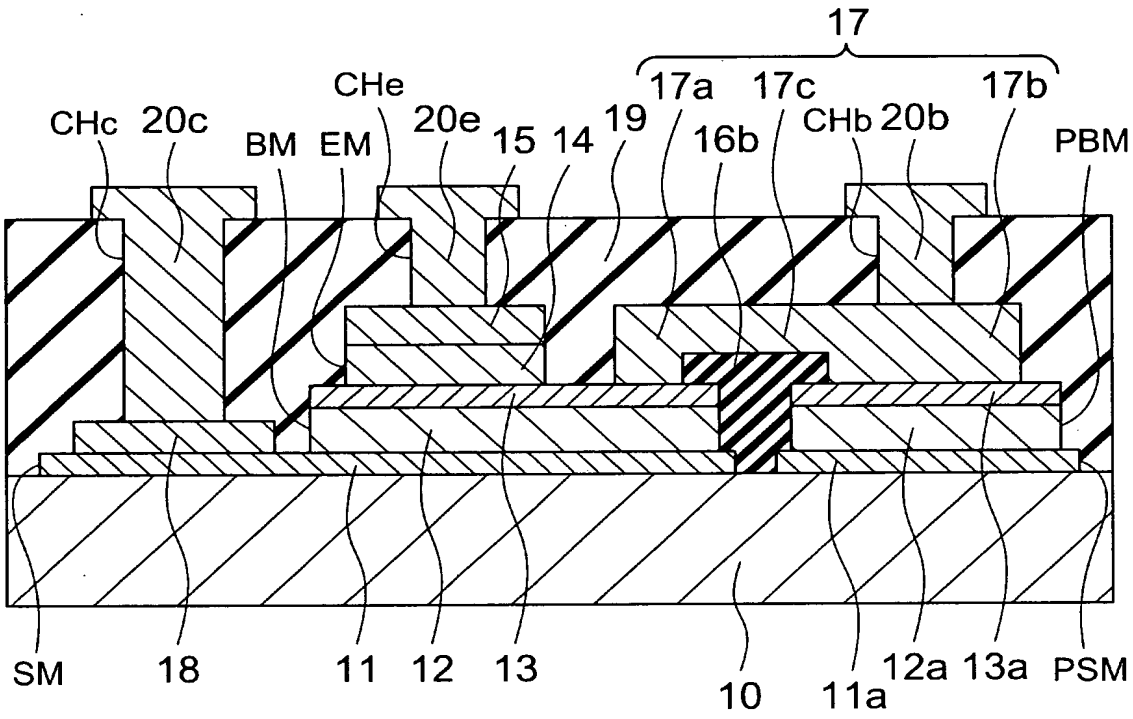

17
CHc
20c
BM
EM
CHe
20e
15
14
19
17a
16b
17c
CHb
20b
17b
PBM
SM
18
11
12
13
10
11a
12a
13a
PSM

FIG. 8A

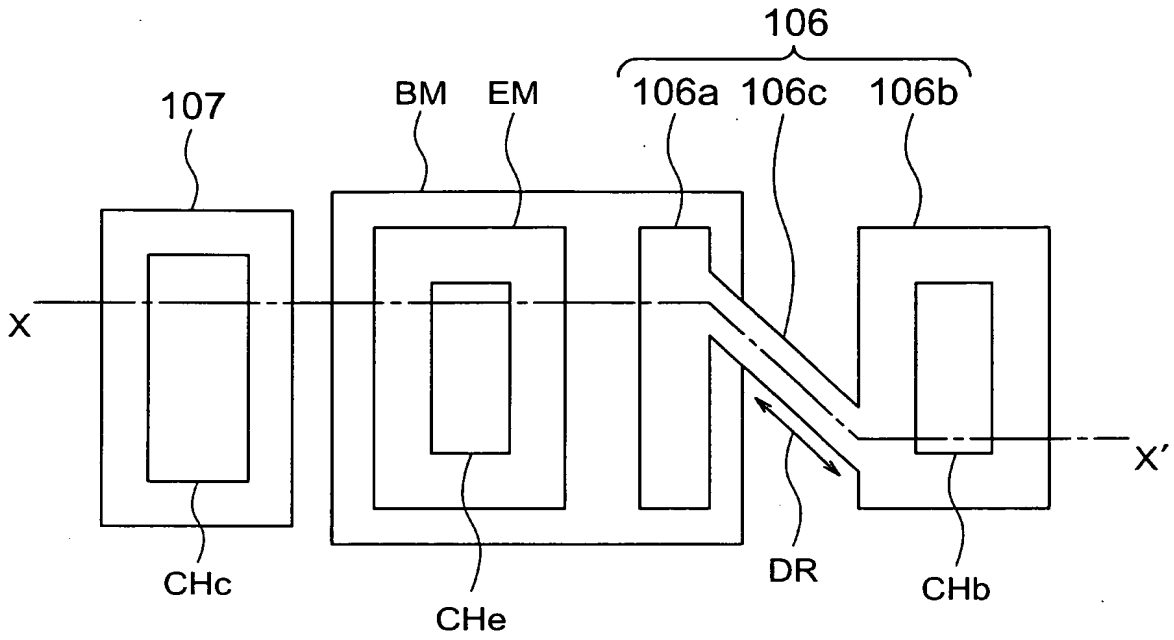

106
107
BM
EM
106a
106c
106b
X
X'
CHc
CHe
DR
CHb

FIG. 8B

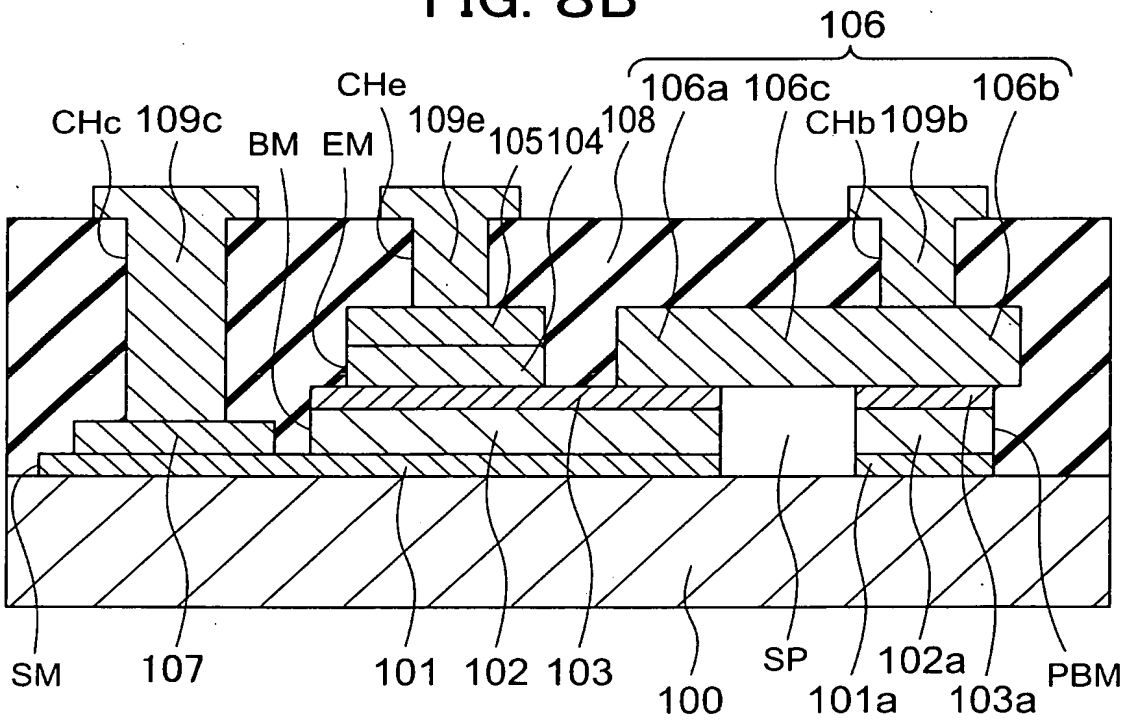

106
CHe
106a
106c
106b
CHc
109c
BM
EM
109e
105
104
108
CHb
109b
SM
107
101
102
103
100
SP
101a
102a
103a
PBM

FIG. 9A

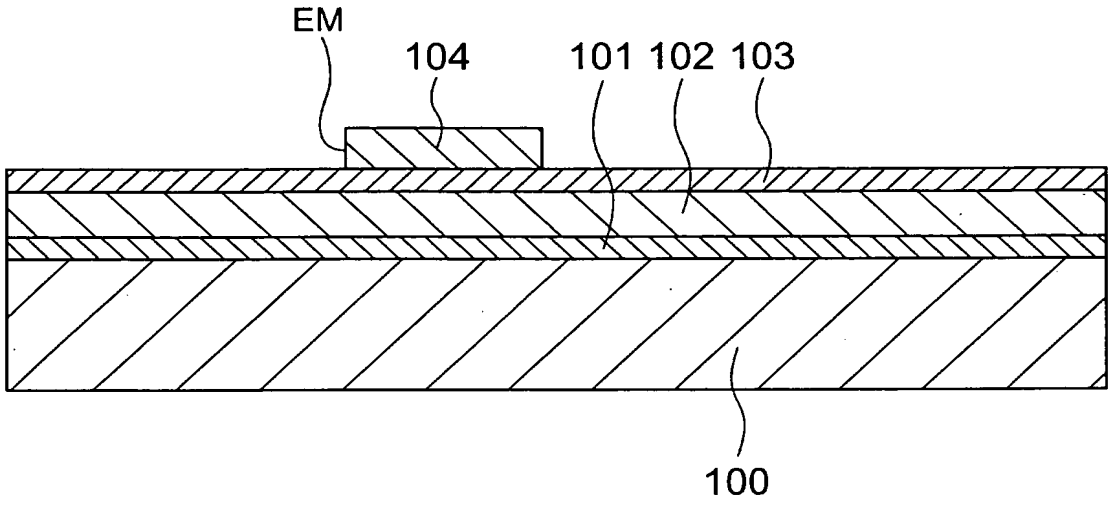

EM
104
101 102 103
100

FIG. 9B

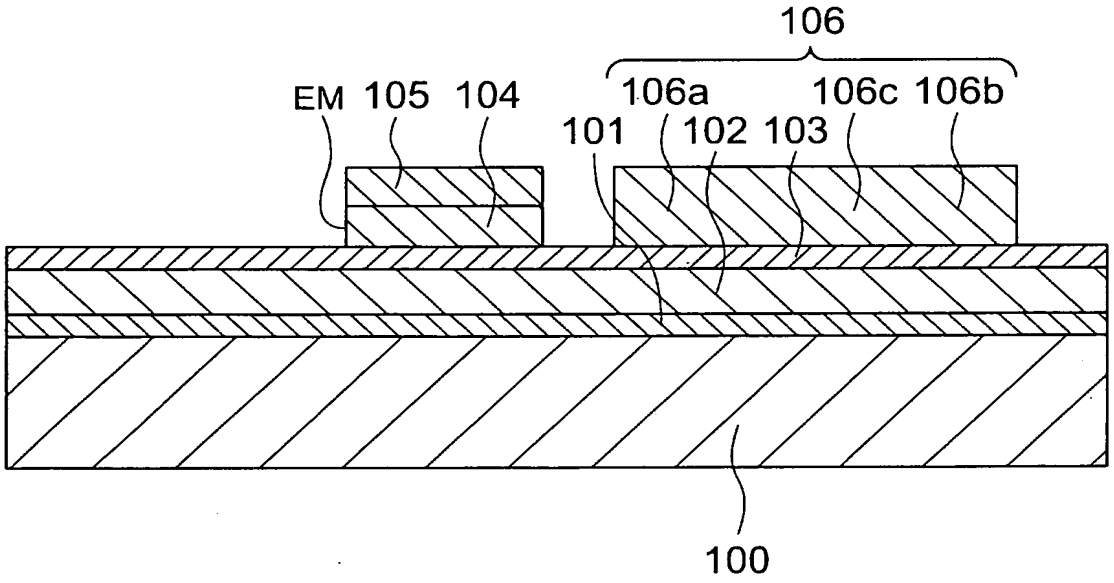

106
EM 105 104
106a
106c 106b
101
102 103
100

FIG. 10A

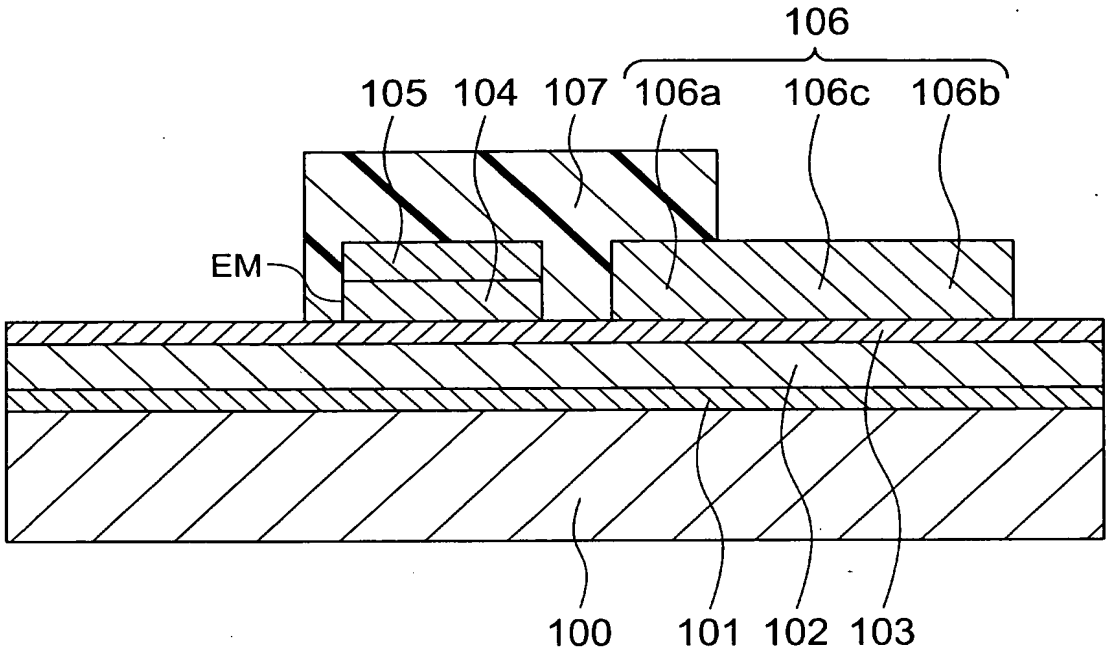
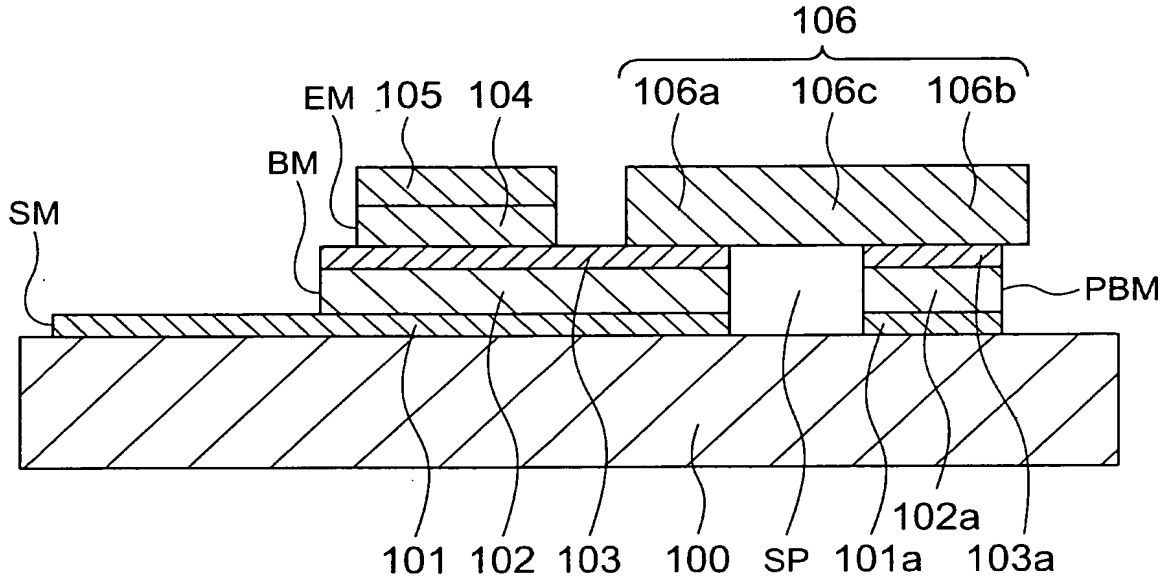


FIG. 10B



[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[PROBLEM] To provide a semiconductor device having a bipolar transistor able to be produced while suppressing the occurrence of mesa shaped abnormalities without restrictions as to the pattern layout, the types of etchant used, etc., and method for producing the same.

[MEANS FOR SOLUTION] The semiconductor device is provided with a semiconductor mesa portion (EM, BM, SM) including a stack of a collector layer 12, a base layer 13, and an emitter layer 14 on a substrate 10 and functioning as an active region of the bipolar transistor, a base contact pad mesa portion (PBM, PSM) separated from the semiconductor mesa portion with a predetermined distance and having the same height as a top surface of the base layer, and a conductor layer 17 integrally formed with a base electrode 17a connected to the base layer, a base contact pad electrode 17b formed on the base contact pad mesa portion in a region other than near edges PBMa of a top surface of the base contact pad mesa portion, and an interconnection portion 17c connecting them.

[SELECTED DRAWING] FIG. 1